

REMARKS

Prior to an examination of the application on the merits, Applicant respectfully requests entry of this preliminary amendment. Claims 1-8 have been amended to place the claims in standard format, as well as to correct grammatical and idiomatic errors. The changes to the claims have not been made for any reason related to the patentability of the claims, and are not intended to limit the scope of the claims.

Attached hereto is a marked-up version of the changes made by the current amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

If there are any other fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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Version with Marking to Show Changes Made

IN THE CLAIMS:

Applicants have amended claims 1 – 8 as follows.

1. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, **the method** comprising [the steps of]:

forming an insulating film spacer [only] on [the] **a** sidewall of **a** conductive layer [patterns] **pattern** at a **contact plug formation** region [where a contact plug will be formed]; and [then]

forming an interlayer dielectric film on [the] **an** entire surface **of the semiconductor device**.

2. (Amended) The method [of forming an interlayer dielectric film in a semiconductor device as claimed in] **according to** claim 1, wherein said conductive layer [patterns are] **pattern comprises one of a** word [lines or] **line and a** bit [lines] **line**.

3. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, **the method** comprising [the steps of]:

forming **a** conductive layer [patterns of a given] pattern and an insulating film spacer on [the sidewalls] **a sidewall** of said conductive layer [patterns] **pattern** through a common process;

removing said insulating film spacer [formed] in a region other than a **contact plug formation** region [where a contact plug will be formed]; and

forming an interlayer dielectric film on [the] **an** entire surface **of the semiconductor device**.

4. (Amended) The method [of forming an interlayer dielectric film in a semiconductor device an claimed in] **according to** claim 3, wherein said conductive layer [patterns are] **pattern comprises one of a** word [lines or] **line and a** bit [lines] **line**.

5. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, **the method** comprising [the steps of]:

forming conductive layer patterns of a given pattern through a common process;

forming an interlayer dielectric film on [the] an entire surface of the semiconductor device; [and]

removing said interlayer dielectric film at a contact plug formation region [where a contact plug will be formed]; and [then]

forming an insulating film spacer on [the] a sidewall of said conductive layer patterns.

6. (Amended) The method [of forming an interlayer dielectric film in a semiconductor device as claimed in] according to claim 5, wherein at least one of said conductive layer patterns [are] comprises one of a word [lines or] line and a bit line.

7. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising [the steps of]:

forming conductive layer patterns [of a given pattern] and an insulating film spacer on [the] a sidewall of said conductive layer patterns through a common process;

burying a conductive material between said conductive layer patterns;

removing said conductive material [only] at a [given] removal region [and remaining] such that said conductive material remains at remaining regions to form a contact plug; and

burying an interlayer dielectric film between said conductive layer patterns at [a] said removal region [from which said conductive material is removed].

8. (Amended) The method [of forming an interlayer dielectric film in a semiconductor device as claimed in] according to claim 7, wherein at least one of said conductive layer patterns [are] comprises one of a word [lines or] line and a bit [lines] line.